REMARKS

Favorable reconsideration of this application in view of the foregoing amendments and remarks to follow is respectfully requested.

Before addressing the specific grounds of rejection raised in the outstanding Office Action, Applicants have amended independent Claims 1 and 14 to positively recite that the claimed conductive back electrode is biased to form an inversion charge layer at a bottom portion of said base region at an interface between said first semiconductor layer and said insulating layer and *said inversion charge layer* serves as an intrinsic collector of said transistor. Support for this amendment to Claims 1 and 14 is found throughout the specification of the instant application. See, in particular, paragraph [0007].

Further, Applicants have amended independent Claims 1 and 14 to positively recite that said base is electrically isolated from said conductive back electrode. Support for this structural characteristics is found in FIGS. 1A – 1D and 9A – 9G and throughout the specification of the instant application. See, in particular, paragraphs [0031], [0036], and [0037].

Since the above amendments to the claims do not introduce new matter into the originally filed application, entry thereof is respectfully requested. Applicants observe that the foregoing amendments to Claims 1 and 14 should be entered and considered in this Response since it clearly defines the inventive structure and in particularly the function of the claimed backgate electrode.

In the outstanding Office Action, Claims 1-14 stand rejected under 35 U.S.C. § 112 for allegedly failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Claims 1-14 also stand rejected under 35 U.S.C. § 103(a) as

allegedly unpatentable over the combined disclosures of U.S. Patent No. 5,352,624 to Miwa et al. ("Miwa et al.") and Japanese Patent No. 05-243255 A to Tsuchiya ("JP '255").

Applicants submit that amended Claims 1 - 14 are both clear and definite and in compliance with the requirements of 35 U.S.C. §112, second paragraph, and as such, addresses the rejection under 35 U.S.C. § 112.

Concerning the 35 U.S.C. § 103(a) rejection, Applicants respectfully submit that Miwa et al. does not teach or suggest Applicants' claimed structure which includes a conductive back electrode that is **electrically isolated from the base** of a bipolar transistor.

Miwa et al. fails to disclose any conductive back gate electrode that is disconnected from a base. Indeed, Miwa et al. discloses that the conductive back gate electrode is removed from the bipolar transistor area. See Col. 41, lines 15-18. Miwa et al. clearly states that the polysilicon film 603b forms a base leading electrode for the bipolar transistor, and a back gate electrode for only the MOSFET. See Col. 41, lines 41-45. In other words, the polysilicon film 603b disclosed by Miwa et al. functions only as a base leading electrode in the bipolar transistor of FIG. 21E, but not as a back gate electrode. In order for the polysilicon film 603b to function as a base leading electrode, **it is necessary that the polysilicon film 603 is electrically connected to the base in the structure disclosed by Miwa et al.** Layer 603b functions as a back gate electrode only in the MOSFET device region, but not in any bipolar device. Therefore, Miwa et al. does not disclose a conductive back electrode 603b for the bipolar transistor that is *electrically isolated* from a base.

In fact, nothing in Miwa et al. teaches or suggests the use of a conductive back electrode as an element electrically isolated from a base in the bipolar transistor of FIG. 21E, much less a bipolar transistor that comprises a conductive back electrode that is biased to form an inversion

charge layer at a bottom portion of a base region at an interface between a first semiconductor layer and an insulating layer and *said an inversion charge layer serves as an intrinsic collector of the claimed transistor.*

Applicants observe that in Miwa et al. the polysilicon layer 603b is the base electrode of the bipolar transistor which is doped to include dopant impurities. See Col. 42, lines 20-33. There is no teaching or suggestion in Miwa et al. that when a bias is applied to the gate electrode 603b an inversion layer forms as presently claimed.

Applicants further observe that in Miwa et al. doped polySi film 603c serves as the collector electrode and, as such, it represents prior art that the claimed invention is trying to circumvent. See paragraph [0007] of the originally filed specification wherein it is stated that the claimed structure includes no impurity doped collector, which is present in Miwa et al.

Since doped poly films 603b and 603c are employed either as a base electrode or as a collector electrode, the doped poly films 603 are electrically connected to, that is, not electrically isolated from, the base of a bipolar transistor. (Applicants note that the base and the collector of a bipolar transistor are electrically connected.) Therefore, **Miwa et al. does not disclose a back gate electrode that is electrically isolated from a base.**

Applicants respectfully submit that the combined references do not teach or suggest Applicants' claimed structure which includes a conductive back electrode that is biased to form an **inversion** charge layer at a bottom portion of a base region at an interface between a first semiconductor layer and an insulating layer wherein said **inversion** charge layer serves as an intrinsic collector of the claimed transistor.

Since a back gate that is electrically isolated from the base of a bipolar transistor is not provided in the structure disclosed by Miwa et al., it is impossible to form any inversion layer

through doped poly films 603b and 603c in any location other than the PN junction between the base and the collector. Since *the bottom portion of the base region at an interface between the first semiconductor layer and the insulating layer* is **not** the PN junction between the base and the collector, it follows that the structure disclosed by Miwa et al. is not capable of forming an inversion layer at the location of *the bottom portion of the base region at an interface between the first semiconductor layer and the insulating layer,* as disclosed and claimed in the present application.

In fact, formation of an inversion layer in a bipolar device is neither taught nor suggested in Miwa et al. in any form since normal bipolar devices do not require an inversion layer.

Therefore, **Miwa et al. does not teach or suggest a structure in which an inversion charge layer is formed** at a bottom portion of said base region at an interface between said first semiconductor layer and said insulating layer.

JP '255 does not alleviate the above mentioned defects in Miwa et al. since the applied secondary reference also does not teach or suggest the inventive structure which includes the claimed back gate electrode that is biased to form **an inversion charge layer** at a bottom portion of a base region at an interface between a first semiconductor layer and an insulating layer which serves as an intrinsic collector of the claimed structure.

Although biasing is mentioned in JP '255 there is no teaching or suggestion of the claimed conductive back gate electrode in which **an inversion charge layer** is formed during biasing. As such, the claimed structures are not rendered obvious by the disclosures of Miwa et al. and JP '255.

Applicants note that JP '255 discloses generation of **a depletion layer** 18 in a boundary between a p-type base region 16 and an SiO_2 film 13. Applicants submit that a depletion layer

and an inversion charge layer are completely different semiconductor structures. A depletion layer is a layer in which the majority charge carriers (holes in a p-doped semiconductor material and electrons in an n-doped semiconductor material) are depleted in a semiconductor structure so that the depletion layer is substantially free of charge carriers. An inversion charge layer, which is also called inversion layer, is a layer in which minority charge carriers (electrons in a p-doped semiconductor material and holes in an n-doped semiconductor material) are formed by an applied bias. Both majority and minority charge carriers are depleted in the depletion layer. Abundant minority carriers are present in the inversion charge layer. Therefore, the depletion layer and the inversion charge layer have fundamentally different electrical characteristics, and disclosure of one type of layer does not teach or suggest use or application of the other type of layer.

As an evidence of the two completely different modes of semiconductor properties between a depletion mode and an inversion charge layer, Applicants submit herewith, a copy of a web page, http://ece-www.colorado.edu/~bart/book/book/chapter6/ch6_2.htm as it was captured at 6:03 p.m. on April 12, 2007, which clearly indicates absence of mobile charge carriers in the depletion mode and the presence of minority charge carriers in the inversion mode.

Therefore, **JP '255 does not teach or suggest formation of an inversion charge layer.**

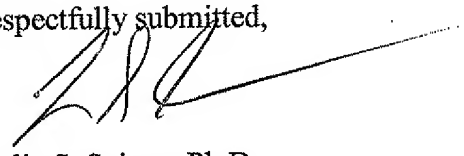
The § 103 rejection also fails because there is no motivation in the applied references which suggest modifying the disclosed structures to include the various elements recited in the claims of the present invention. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification

obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. § 103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

In view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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Chapter 6: MOS Capacitors

6.2. Structure and principle of operation

The MOS capacitor consists of a Metal-Oxide-Semiconductor structure as illustrated by Figure 6.2.1. Shown is the semiconductor substrate with a thin oxide layer and a top metal contact, referred to as the gate. A second metal layer forms an Ohmic contact to the back of the semiconductor and is called the bulk contact. The structure shown has a *p*-type substrate. We will refer to this as an *n*-type MOS or nMOS capacitor since the inversion layer - as discussed in section 6.6.4 - contains electrons.

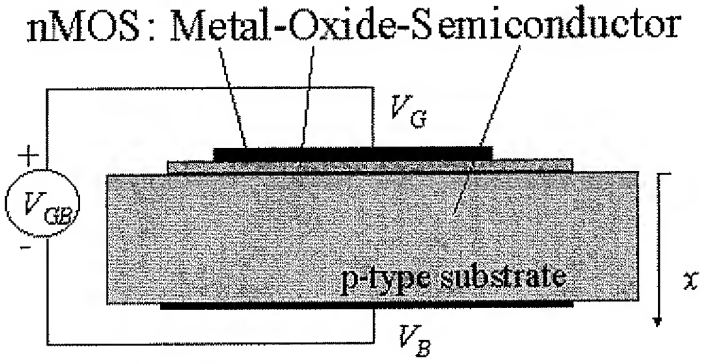

Figure 6.2.1: MOS capacitance structure

To understand the different bias modes of an MOS capacitor we now consider three different bias voltages. One below the flatband voltage, V_{FB}, a second between the flatband voltage and the threshold voltage, V_T, and finally one larger than the threshold voltage. These bias regimes are called the accumulation, depletion and inversion mode of operation. These three modes as well as the charge distributions associated with each of them are shown in Figure 6.2.2.

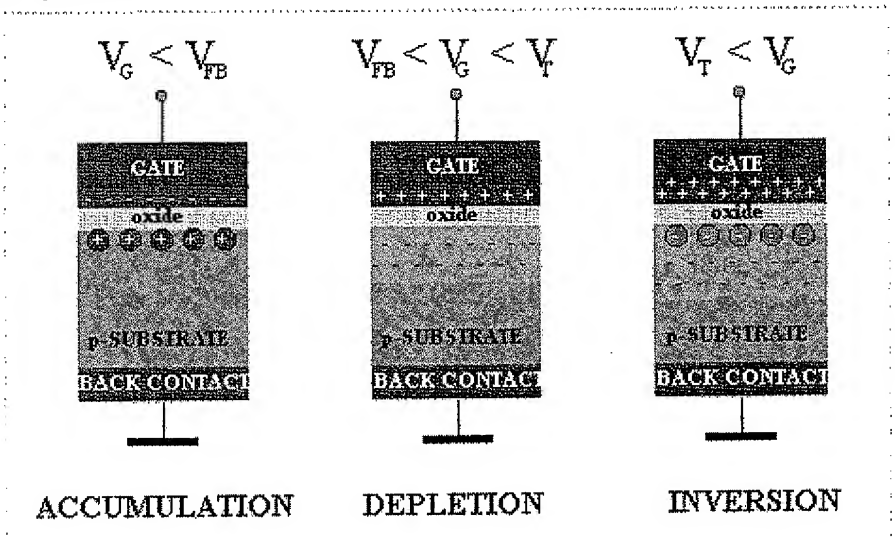

Figure 6.2.2.: Charges in an *n*-type Metal-Oxide-Semiconductor structure (*p*-type substrate) under accumulation, depletion and inversion conditions.

Accumulation occurs typically for negative voltages where the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Depletion occurs for positive voltages. The positive charge on the gate pushes the mobile holes into the substrate. Therefore, the semiconductor is depleted of mobile carriers at the interface and a negative charge, due to the ionized acceptor ions, is left in the space charge region. The voltage separating the accumulation and depletion regime is referred to as the *flatband voltage*, V_{FB}. Inversion occurs at voltages beyond the threshold voltage. In inversion, there exists a negatively charged inversion layer at the oxide-semiconductor interface in addition to the depletion-layer. This inversion layer is due to the minority carriers that are attracted to the interface by the positive gate voltage.

The energy band diagram of an *n*-MOS capacitor biased in inversion is shown in Figure 6.2.3. The oxide is modeled as a semiconductor with a very large bandgap and blocks any flow of carriers between the semiconductor and the gate metal. The band bending in the semiconductor is consistent with the presence of a depletion layer. At the semiconductor-oxide interface, the Fermi energy is close to the conduction band edge as expected when a high density of electrons is present. The semiconductor remains in thermal equilibrium even when a voltage is applied to the gate. The presence of an electric field does not automatically lead to a non-equilibrium condition, as was also the case for a p-n diode with zero bias.

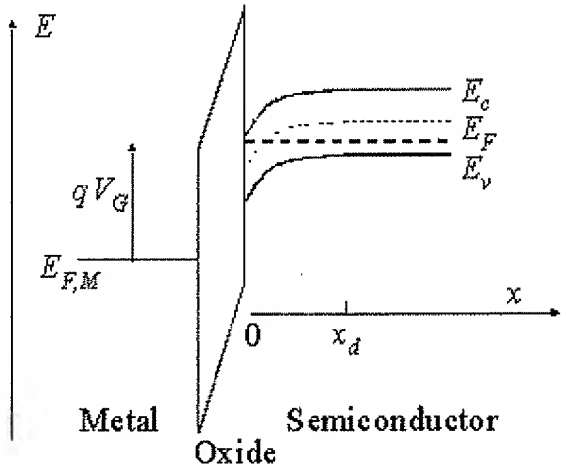

Figure 6.2.3: Energy band diagram of an MOS structure biased in inversion.

In the next sections, we discuss the four modes of operation of an MOS structure: Flatband, Depletion, Inversion and Accumulation. Flatband conditions exist when no charge is present in the semiconductor so that the silicon energy band is flat. Initially we will assume that this occurs at zero gate bias. Later we will consider the actual flatband voltage in more detail. Surface depletion occurs when the holes in the substrate are pushed away by a positive gate voltage. A more positive voltage also attracts electrons (the minority carriers) to the surface, which form the so-called inversion layer. Under negative gate bias, one attracts holes from the *p*-type substrate to the surface, yielding accumulation.

6.2.1. Flatband diagram

The flatband diagram is by far the easiest energy band diagram. The term flatband refers to fact that the energy band diagram of the semiconductor is flat, which implies that no charge exists in the semiconductor. The flatband diagram of an aluminum-silicon dioxide-silicon MOS structure is shown in Figure 6.2.4. Note that a voltage, V_{FB}, must be applied to obtain this flat band diagram. Indicated on the figure is also the work function of the aluminum gate, Φ_M, the electron affinity of the oxide, χ_{oxide}, and that of silicon, χ, as well as the bandgap energy of silicon, E_g. The bandgap energy of the oxide is quoted in the literature to be between 8 and 9 electron volt. The reader should also realize that the oxide is an amorphous material and the use of semiconductor parameters for such material can justifiably be questioned.

The flatband voltage is obtained when the applied gate voltage equals the workfunction difference between the gate metal and the semiconductor. If there is a fixed charge in the oxide and/or at the oxide-silicon interface, the expression for the flatband voltage must be modified accordingly.

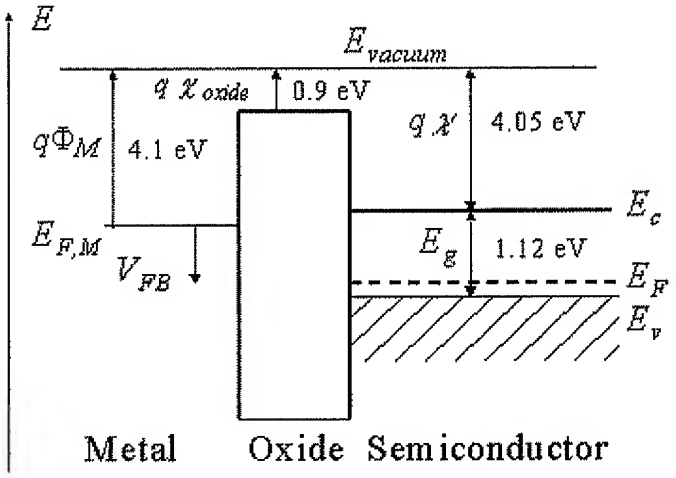

Figure 6.2.4: Flatband energy diagram of a metal-oxide-semiconductor (MOS) structure consisting of an aluminum metal, silicon dioxide and silicon.

6.2.2. Accumulation

Accumulation occurs when one applies a voltage less than the flatband voltage. The negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Only a small amount of band bending is needed to build up the accumulation charge so that almost all of the potential variation is within the oxide.

6.2.3. Depletion

As a more positive voltage than the flatband voltage is applied, a negative charge builds up in the semiconductor. Initially this charge is due to the depletion of the semiconductor starting from the oxide-semiconductor interface. The depletion layer width further increases with increasing gate voltage.

6.2.4. Inversion

As the potential across the semiconductor increases beyond twice the bulk potential, another type of negative charge emerges at the oxide-semiconductor interface: this charge is due to minority carriers, which form a so-called inversion layer. As one further increases the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential.

Boulder, December 2004